PVP 20

Code: 20CS3303

II B.Tech - I Semester – Regular Examinations - FEBRUARY 2022

COMPUTER ORGANIZATION AND ARCHITECTURE
(COMPUTER SCIENCE & ENGINEERING)

Duration: 3 hours Max. Marks: 70

Note: 1. This paper contains questions from 5 units of Syllabus. Each unit carries 14 marks and have an internal choice of Questions.
2. All parts of Question must be answered in one place.

UNIT – I

1. a) Design one stage of Arithmetic Logic Shift unit. 7 M
   b) Design a 4-bit arithmetic circuit using four full adders. 7 M

OR

2. a) With a neat sketch, explain 4-bit combinational circuit shifter. 7 M
   b) Design and explain 4-bit adder-subtractor. 7 M

UNIT – II

3. a) Explain the three different types of instruction formats used in basic computer. 7 M
   b) Demonstrate the usage of interrupt cycle during the execution of Input/Output instruction. 7 M

OR

4. a) Draw the flowchart for instruction cycle representing all the phases. 7 M
   b) What is instruction set completeness? 7 M

UNIT-III

5. a) What are the three types of CPU organizations and explain with an example? 7 M

   b) Discuss logical and bit manipulation instructions. 7 M

OR

6. a) Evaluate the arithmetic statement X = (A + B) * (C + D) using zero, one, two and three address instructions. 7 M

   b) Translate the following symbolic program for the fetch routine to binary micro program? 7 M

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            ORG 64
FETCH :   PCTAR          U   JMP  NEXT
          READ, INCPC    U   JMP NEXT
          DRTAR          U   MAP
```

UNIT – IV

7. a) Explain about an associative memory page table. 7 M

   b) What is memory hierarchy? Explain with a block diagram. What is the reason for not having one large memory unit for storing all information at one place? 7 M

OR

8. a) A digital computer has a memory unit of 64K + 16 and a cache memory of 1K words. Cache uses direct mapping with a block size of 4 words. 7 M

   i) How many bits are there in the tag, index, block and word fields of the address format?

   ii) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit.

   iii) How many blocks can the cache accommodate?

b) Show the step-by-step multiplication process using Booth algorithm for the binary numbers (+15) X (-13) 7 M

UNIT – V

9. a) What is DMA? Draw the block diagram of DMA controller? 7 M

b) What is meant by pipelining? Why do we require instruction pipelining? 7 M

OR

10. a) Determine the number of clock cycles that it takes to process 200 tasks in a six-segment pipeline. 7 M

b) Explain Daisy chaining priority interrupt. 7 M